Amendments to the Claims

1. (Cancelled) A method of fabricating a memory cell, said method comprising the steps of:

forming a conductive layer in a trench of an insulating layer;

forming a first dielectric layer having a top surface over said conductive layer and said insulating layer;

forming an opening in said first dielectric layer over said conductive layer;

forming a first magnetic layer within said opening and over said first dielectric layer;

forming a nonmagnetic layer over said first magnetic layer;

forming a second magnetic layer over said nonmagnetic layer;

forming a second dielectric layer over said second magnetic layer; and

planarizing said first magnetic layer, nonmagnetic layer, second magnetic layer, and said second dielectric layer down to said top surface to form said memory cell.

2-28. (Previously Cancelled)

29. (New) A magnetic random access memory cell, said memory cell comprising:

a first magnetic layer over a conductive layer, said first magnetic layer comprising a first plurality of magnetic multilayer films;

a nonmagnetic tunnel barrier layer over said first magnetic layer; and

a second magnetic layer over said nonmagnetic tunnel barrier layer, said second magnetic layer comprising a second plurality of magnetic multilayer films.

30. (New) The memory cell of claim 29, wherein said first magnetic layer is a pinned layer.

31. (New) The memory cell of claim 30, wherein said pinned layer comprises a plurality of layers to produce a ferromagnetic pinned layer.

32. (New) The memory cell of claim 29, wherein said second magnetic layer is a sense layer.

33. (New) The memory cell of claim 32, wherein said sense layer comprises a plurality of layers to produce a ferromagnetic sense layer.

34. (New) The memory cell of claim 29, wherein said nonmagnetic tunnel barrier layer comprises aluminum oxide.

35. (New) The memory cell of claim 34, wherein said aluminum oxide has a thickness of about 5 to 25 Angstroms.

36. (New) The memory cell of claim 29, wherein said nonmagnetic tunnel barrier layer comprises a material selected from the group consisting of copper, titanium oxide, magnesium oxide, silicon oxide and aluminum nitride.

37. (New) The memory cell of claim 29, wherein said conductive layer is selected from the group consisting of copper, aluminum, tungsten and gold.

38. (New) The memory cell of claim 29, wherein said first plurality of magnetic multilayer films comprises a first tantalum layer, a first nickel-iron layer, a manganese-iron layer, and a second nickel-iron layer.

39. (New) The memory cell of claim 29, wherein said second plurality of magnetic multilayer films comprises a third nickel-iron layer, a tungsten nitrogen layer and a second tantalum layer.

40. (New) The memory cell of claim 29, wherein said memory cell is coupled to at least one word line.

41. (New) A memory circuit, said memory circuit comprising:

a plurality of memory cells, each memory cell comprising:

a first magnetic layer over a conductive layer, said first magnetic layer comprising a first plurality of magnetic multilayer films;

a nonmagnetic tunnel barrier layer over said first magnetic layer; and

a second magnetic layer over said nonmagnetic tunnel barrier layer, said second magnetic layer comprising a second plurality of magnetic multilayer films.

42. (New) A processor system comprising at least one a memory circuit, wherein said at least one a memory circuit comprises at least one memory cell according to claim 29.